UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.usplo.gov

| APPLICATION NO.          | FILING DATE                       | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--------------------------|-----------------------------------|----------------------|---------------------|------------------|
| 10/743,079               | 12/23/2003                        | Uming Ko             | TI-29632.1          | 8111             |
| <del></del>              | 7590 11/06/200<br>RUMENTS INCORPO | EXAMINER             |                     |                  |
| P O BOX 655474, M/S 3999 |                                   |                      | FULK, STEVEN J      |                  |
| DALLAS, TX 75265         |                                   |                      | ART UNIT            | PAPER NUMBER     |
|                          |                                   |                      | 2891                |                  |
|                          |                                   |                      |                     |                  |
|                          |                                   |                      | NOTIFICATION DATE   | DELIVERY MODE    |
|                          |                                   |                      | 11/06/2007          | ELECTRONIC       |

# Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com uspto@dlemail.itg.ti.com

|  | Application No.  | Applicant(s) |  |  |  |
|--|--|--------------|--|--|--|
| •  | 10/743,079   | KO, UMING    |  |  |  |
| Office Action Summary  | Examiner   | Art Unit     |  |  |  |
|  | Steven J. Fulk   | 2891         |  |  |  |
| The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply   |  |              |  |  |  |
| A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). |  |              |  |  |  |
| Status   |  |              |  |  |  |
| <ol> <li>Responsive to communication(s) filed on 9/17/07.</li> <li>This action is FINAL.</li> <li>Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.</li> </ol>   |  |              |  |  |  |
| Disposition of Claims  |  |              |  |  |  |
| 4)  Claim(s) 42-53 is/are pending in the application.  4a) Of the above claim(s) is/are withdrawn from consideration.  5)  Claim(s) 43,44,46,47,49,50,52 and 53 is/are allowed.  6)  Claim(s) 42,45,48 and 51 is/are rejected.  7)  Claim(s) is/are objected to.  8)  Claim(s) are subject to restriction and/or election requirement.  Application Papers  9)  The specification is objected to by the Examiner.  10)  The drawing(s) filed on 24 May 2005 is/are: a)  accepted or b)  objected to by the Examiner.  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  |  |              |  |  |  |
| 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.   |  |              |  |  |  |
| Priority under 35 U.S.C. § 119   |  |              |  |  |  |
| <ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>   |  |              |  |  |  |
| Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO/SB/08)  Paper No(s)/Mail Date   | 4)  Interview Summary Paper No(s)/Mail D  5)  Notice of Informal F  6)  Other: | ate          |  |  |  |

10/743,079 Art Unit: 2891

#### **DETAILED ACTION**

## Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- 2. Claims 42, 45, 48, and 51 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (AAPA).

AAPA discloses a semiconductor wafer comprising a plurality of integrated circuits and a method of fabricating the semiconductor wafer comprising: providing a plurality of integrated circuits (fig. 3, 10), each of the integrated circuits separated from the other of the integrated circuits by a scribe region (20; Specification, paragraph 17) at the periphery of each the integrated circuit; and providing in each of the integrated circuits: a centrally disposed core region (40); at least one bond pad (12) disposed between the core region and the scribe region; an electrostatic discharge device (14); and an I/O buffer (16) disposed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region (fig. 3; turned 90° shows buffer 16 between scribe 20 and core 40, as well as laterally positioned to the bond pad 12 relative to scribe and core).

10/743,079 Art Unit: 2891

## Response to Arguments

3. Applicant's arguments filed with respect to claims 42, 45, 48, and 51 have been fully considered but they are not persuasive. Applicant argues that AAPA does not teach the I/O buffer to be on the side of the bond pad relative to the core and scribe regions. This argument is not found persuasive because the locations of the elements are relative to the orientation of fig 3. When figure 3 is turned 90°, the elements are then aligned as recited by the claims. Specifically, the core and scribe regions are on the side of the bond pad when turned 90°, therefore I/O buffer is on the side of the bond pad relative to the core and scribe regions.

## Allowable Subject Matter

- 4. Claims 43, 44, 46, 47, 49, 50, 52 and 53 are allowed.
- 5. The following is an examiner's statement of reasons for allowance: a search of the prior art failed to disclose or reasonably suggest a semiconductor wafer and method of fabricating thereof, comprising providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits: a centrally disposed core region; at least one bond pad disposed between said core region and said scribe region; an electrostatic discharge device disposed at least partially beneath said bond pad; and an I/O buffer disposed between said scribe region and said core region, as recited in claims 43, 46, 49, and 52.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should

10/743,079 Art Unit: 2891

preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

#### Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10/743,079

Art Unit: 2891

Page 5

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SSF

Steven J. Fulk Patent Examiner Art Unit 2891

October 31, 2007

B. WILLIAM BAUMEISTER

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800